parallel pipelined hardware of said at least one specialized processing module and said microprocessor of said general processing module to perform predetermined specialized processing operations on the input stream of data; and

a global control bus which provides control data to/from said hardware control library of said general processing module from/to said at least one specialized processing module separate from said stream of input data to be processed by said general processing module and said at least one specialized processing module.

31. (Newly Added) The system of claim 1, wherein the plurality of parallel pipelined video hardware components are configured to perform the different video processing operations ~~synchronously or~~ asynchronously.

REMARKS

Claims 1-20 and 22-31 are pending in the above identified application.

Claims 1, 20-22, 24, 25, 27, 28 and 30 were rejected under 35 U.S.C. §103 (a) as being obvious in view of Gove et al. (hereinafter Gove) and Katsura et al. (hereinafter Katsura). With respect to claim 1, this ground for rejection is traversed. With respect to claims 20, 22, 24, 25, 27, 28 and 30 this ground for rejection is overcome by the amendments to claims 20 and 27. With respect to claim 21, this ground for rejection is overcome by the cancellation of claim 21. In particular, neither Gove, Katsura nor any combination thereof discloses or suggests:

> a global video bus which establishes a direct connection between the processing module and said at least one video processing module to route the video data between said processing module and said at least one video processing module; and

as set forth in claim 1,

> connecting said global control bus and said global video bus to at least one video processing module which contains parallel pipelined video hardware that is responsive to said configuration data to provide respectively different video processing operations on the video data, the video processing module being configured to perform the different video processing operations concurrently; ... and
>
> associating video timing signals synchronized to a system clock signal with the video data, wherein each video processing module routes the video data and associated timing signals from any one of the multiple concurrent video processing operations to any one or more of the multiple concurrent video processing operations said timing signals indicating when the video data represents active video information

as set forth in amended claim 20 or

> at least one specialized processing module which contains a plurality of parallel pipelined hardware components that are programmable to provide respectively different, synchronous or asynchronous specialized processing operations on an input stream of data;

as set forth in amended claim 27. Basis for the amendments to claims 20 and 27 may be found in claim 21 and in the specification at page 14, lines 8-31.

Gove discloses a crossbar switch 20 that connects a master processor, several parallel processors and a transfer processor to a group of shared memories 10. The processors can only transfer data with each other through the memories 10. (See col. 11, line 66 through col. 12, line 14). In addition, Gove discloses a MIMD communication/synchronization network 40 that connects the various processors to communicate synchronization

signals among the processors. (See col. 10, lines 2-5, col. 42, lines 12-24 and Col. 40, lines 23-34). Only synchronization signals are available on the bus 40. Image and graphic data and program data are transferred via the crossbar switch 20 and only between one of the processors 12, 100, 101, 102 and 103 and the memory 10. (See Figs. 4 and 21 and col. 19, line 65 - col. 20, line 7).

Katsura concerns a graphic processing system that includes a CPU and a single graphics processor. The Graphics processor is connected to a main memory and to a specialized frame memory via a reconfigurable bus. Katsura does not disclose or suggest that the graphics processor "contains a plurality of parallel pipelined video hardware components" or "a global video bus which establishes a direct connection between the processing module and said at least one video processing module to route the video data between said processing module and said at least one video processing module" as required by claim 1. Katsura does disclose that the graphics processor may perform pipelined operations but does not disclose or suggest any "parallel pipelined video hardware components." In addition, Katsura discloses only that the graphics processor may access the main memory and not that data may be transferred from the CPU to the graphics processor.

Even if Katsura did disclose transferring data between the CPU and the graphics processor via the data bus, it is not apparent how Katsura would be combined with Gove. The crossbar switch used by Gove is fundamentally different from the simple bus used by Katsura. One motivation stated by Gove for using the crossbar switch is to avoid conflicts in access among the separate processors (see column 3, lines 9-14). Combining Gove with Katsura would be contrary to this motivation. Accordingly, Gove teaches away from substituting a data bus for the crossbar switch.

Because neither Gove nor Katsura disclose or suggest "a global video bus which establishes a direct connection between the processing module and said at least one video processing module to route the video data between said processing module and said at least one video processing module," Claim 1 is not subject to rejection under 35 U.S.C. § 103(a) in view of Gove and Katsura.

With regard to claims 20 and 27, neither Gove nor Katsura disclose or suggest a "video processing module being configured to perform the different video processing operations concurrently" or that video timing signals are associated with the video data, the timing signals indicating "when the video data represents active video information" In the Office Action, it is contended that the horizontal and vertical synchronization signals disclosed by Gove meet this limitation. In addition, the Office Action contends that the video data that is transmitted via the crossbar switch inherently includes timing and synchronization signals. Even if this were true, however, there is no disclosure in Gove or in Katsura to render obvious the requirement in claim 20 that the timing signals indicate when the video data represents active video information. The "inherent" timing signals in Gove or Katsura can only be simple clock signals which indicate sample timing. These timing signals can not indicate whether a particular sample represents active video data. The horizontal and vertical synchronization signals, if they are transmitted by Gove, would be transmitted as data, not as separate but associated timing signals as required by claim 27. Accordingly, claim 20 is not subject to rejection under 35 U.S.C. § 103(a) in view of Gove and Katsura.

With regard to claim 27, neither Gove nor Katusra disclose or suggest that the "plurality of parallel pipelined hardware components" in the video processing module are "programmable to provide respectively different, synchronous or asynchronous specialized processing operations on

an input stream of data" as required by claim 7. Both Gove and Katsura describe only synchronous processing operations. Accordingly, claim 27 is not subject to rejection under 35 U.S.C. § 103(a) in view of Gove and Katsura.

Claims 22, 24 and 25 depend from claim 20 and are not subject to rejection under 35 U.S.C. § 103(a) in view of Gove and Katsura for at least the same reasons as claim 20. Claims 28 and 30 depend from claim 27 and are not subject to rejection under 35 U.S.C. § 103(a) in view of Gove and Katsura for at least the same reasons as claim 27.

In addition, with regard to claim 28, in the Office Action, the crossbar switch disclosed by Gove is read as meeting the crosspoint switch limitation in claim 28. The crossbar switch, however, has previously been read as meeting the global video bus limitation of claim 27 from which claim 28 depends. The crossbar switch disclosed by Gove does not perform the functions of both the global video bus and the crosspoint switch. Katsura does not disclose or suggest any apparatus that would meet the limitation of the crosspoint switch. Accordingly, claim 28 is not subject to rejection under 35 U.S.C. § 103(a) in view of Gove and Katsura.

Claims 12-19, 23 and 29 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Gove and Katsura in view of Trimberger. With regard to claims 12-19 and 29, this ground for rejection is overcome by the amendment to claim 12 that makes claim 12 depend from newly added claim 31 and by the amendments to claim 29. Neither Gove, Katsura, Trimberger nor any combination thereof disclose or suggest a "plurality of parallel pipelined video hardware components [that] are configured to perform the different video processing operations synchronously or asynchronously" as required by newly added claim 31. Amended claim 29 includes similar recitations. As set forth above, Gove discloses a master processor and a plurality of parallel processors but all processes run

synchronously using the communications and synchronization network 40. Katsura does not disclose multiple parallel processors. Consequently, it can not disclose a plurality of parallel pipelined video hardware components that are configured to perform different video processing operations and, so, it can not disclose such a plurality of hardware components that operate either synchronously or asynchronously. Trimberger describes a microprocessor emulated FPGA. It also does not disclose the combination of a master processor and multiple parallel pipelined video hardware components. Consequently, it can not disclose or suggest the same combination where the video hardware components perform different video processing operations asynchronously.

Accordingly, claims 12-19 and 29 are not subject to rejection under 35 U.S.C. §103(a) in view of Gove and Katsura in view of Trimberger.

With regard to claim 23, it depends from claim 20 and is not subject to rejection under 35 U.S.C. §103(a) in view of Gove and Katsura in view of Trimberger for at least the same reason that it is not obvious in view of Gove and Katsura. As set forth above, neither Gove nor Katsura disclose or suggest a "video processing module being configured to perform the different video processing operations concurrently" or that video timing signals are associated with the video data, the timing signals indicating "when the video data represents active video information." Trimberger only describes a microprocessor emulated FPGA and does not add the material that is missing from Gove and Katsura. Accordingly, claim 23 is not subject to rejection under 35 U.S.C. § 103(a) in view of Gove, Katsura and Trimberger.

Applicants appreciate the indication in the Office Action that claims 2-11 and 26 are rejected only because they are dependent from rejected base claims but would be allowable if rewritten to be independent in

form, including all of the limitations of their base claim. Claim 2 has been rewritten to include all of the limitations of claim 1. Claims 3-11 depend from claim 2, accordingly, claims 2-11 are in condition for allowance. Claim 26 depends from claim 20 which is in condition for allowance. Accordingly, claim 26 is also in condition for allowance.

In view of the foregoing amendments and remarks, Applicants respectfully request that the rejection of claims 1-20 and 22-30 be reconsidered and withdrawn and that newly added claim 31 be allowed.

Respectfully Submitted,

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Kenneth N. Nigon